AMENDMENT TO THE CLAIMS

This listing of claims will replace all prior versions of claims in the application.

Listing of Claims:

1. (currently amended) A processor comprising:

an execution circuit configured to execute an instruction, the execution circuit including at least a first subcircuit and a second subcircuit;

an issue circuit coupled to the execution circuit, wherein the issue circuit is configured to issue an instruction to the execution circuit, ~~and wherein the issue circuit is configured~~ the issue circuit including a counter which is initialized to count a latency value of the instruction at issuance of the instruction and to generate a control signal ~~responsive to whether or not the instruction is issued~~ to the execution circuit to control clock gating in the execution unit responsive to the latency value initialized in the counter; and

a ~~clock tree for~~ clocking circuitry ~~in the processor, wherein a portion of the clock tree supplies~~ to provide a plurality of clocks ~~to~~ for the execution circuit, the plurality of clocks including at least a first clock clocking the first subcircuit and at least a second clock clocking the second subcircuit, the ~~portion of the clock tree~~ clocking circuitry coupled to receive the control signal for collectively conditionally gating the plurality of clocks, and ~~wherein the portion of the clock tree is configured~~ to individually conditionally gate at least some of the plurality of clocks responsive to activity in the respective subcircuits of the execution circuit.

2. (currently amended) The processor as recited in claim 1 wherein the issue circuit is configured to generate the control signal ~~in a state not gating~~ to not gate the plurality of clocks for a ~~plurality~~ particular number of consecutive clock cycles in response to issuing the instruction.

3. (currently amended) The processor as recited in claim 2 wherein the ~~clock tree~~ clocking circuit is configured to individually gate the plurality of clocks on a clock cycle by clock cycle basis.

4. (canceled)

5. (currently amended) The processor as recited in claim ~~4~~ 1 wherein the issue circuit is configured to reinitialize the counter responsive to issuing a second instruction to the execution circuit.

6. (currently amended) The processor as recited in claim ~~4~~ 1 wherein the issue circuit is configured to decrement the counter each clock cycle, and wherein the issue circuit is configured to continue generating the control signal ~~in the state not gating~~ to not gate the plurality of clocks responsive to the counter having a non-zero value.

7. (currently amended) The processor as recited in claim ~~4~~ 1 wherein the issue circuit is configured to initialize the counter based on a latency of the execution circuit in executing the instruction.

8. (currently amended) The processor as recited in claim 7 wherein the counter is initialized to a number of clock cycles greater than or equal to the latency value of the instruction.

9. (currently amended) The processor as recited in claim ~~8~~ 7 wherein the counter is initialized to a number of clock cycles equal to the latency value of the instruction.

10. (currently amended) The processor as recited in claim 1 wherein the execution circuit ~~comprises~~ is a floating point unit.

11. (currently amended) The processor as recited in claim 10 wherein the first subcircuit ~~comprises~~ includes an adder circuit and wherein the second subcircuit ~~comprises~~ includes a multiplier circuit.

12. (currently amended) The processor as recited in claim 11 wherein the floating point

unit further ~~comprising a third subcircuit~~ includes an approximation circuit clocked by at least a third clock of the plurality of clocks~~, wherein the third subcircuit includes an approximation circuit~~.

13. (currently amended) The processor as recited in claim 1 wherein the execution circuit ~~comprises circuitry for executing~~ is to execute a load/store instruction.

14. (currently amended) The processor as recited in claim 1 wherein the first subcircuit ~~comprises~~ includes a load/store unit and wherein the second subcircuit ~~comprises~~ includes a data cache.

15. (currently amended) An apparatus comprising:

a first circuit, including at least a first subcircuit and a second subcircuit, to execute an instruction and; ~~and~~

a second circuit coupled to issue an instruction to the first circuit, wherein the second circuit includes a counter circuit which is initialized to count a latency value of the instruction at issuance of the instruction and to generate a control signal to the first circuit to control clock gating in the first circuit responsive to the latency value initialized in the counter circuit; and

~~a clock tree having~~ clocking circuit to receive a clock input~~, a~~ and the control ~~input~~ signal, and to output a plurality of clock outputs, ~~at least~~ in which a first clock output of the plurality of clock outputs is coupled to the first subcircuit and ~~at least~~ a second clock output of the plurality of clock outputs is coupled to the second subcircuit~~;~~, wherein the plurality of clock outputs are collectively conditionally gated from the clock input responsive to the control ~~input;~~ signal and wherein at least some of the plurality of clock outputs are individually conditionally gated from the clock input further responsive to ~~circuitry monitoring~~ activity in the respective subcircuits.

16. (canceled)

17. (currently amended) The apparatus as recited in claim 15 wherein the ~~clock tree~~

~~comprises~~ clocking circuit includes a plurality of levels of clock buffer circuitry, and wherein a first level of the plurality of levels includes one or more logic gates which combine the clock input and the control signal input.

18. (currently amended) The apparatus as recited in claim 17 wherein a number of ~~the plurality of~~ levels is ~~4~~ four.

19. (canceled)

20. (currently amended) A carrier medium comprising one or more data structures representing:

a first circuit, including at least a first subcircuit and a second subcircuit, to execute an instruction and; ~~and~~

a second circuit coupled to issue an instruction to the first circuit, wherein the second circuit includes a counter circuit which is initialized to count a latency value of the instruction at issuance of the instruction and to generate a control signal to the first circuit to control clock gating in the first circuit responsive to the latency value initialized in the counter circuit; and

a ~~clock tree having~~ clocking circuit to receive a clock input, ~~a~~ and the control ~~input~~ signal, and to output a plurality of clock outputs, ~~at least~~ in which a first clock output of the plurality of clock outputs is coupled to the first subcircuit and ~~at least~~ a second clock output of the plurality of clock outputs is coupled to the second subcircuit;, wherein the plurality of clock outputs are collectively conditionally gated from the clock input responsive to the control ~~input;~~ signal and wherein at least some of the plurality of clock outputs are individually conditionally gated from the clock input further responsive to ~~circuitry monitoring~~ activity in the respective subcircuits.